Synthesizer End Decade (635-0657-001)

Rockwell International

instructions

Collins Telecommunications Products Division

Printed in USA

523-0767973-101211
1 June 1977
1st Revision, 1 June 1978

1. DESCRIPTION

Synthesizer End Decade 635-0657-001, shown in figure 1, is a 2-layer planar card with a 20-pin edge-on connector (2-layers, 10 pins each).

The synthesizer end decade consists of a logic circuit, a low-pass filter circuit, a vco circuit, a loss-of-lock (LOL) monitor circuit, and a divide-by-10 output circuit.

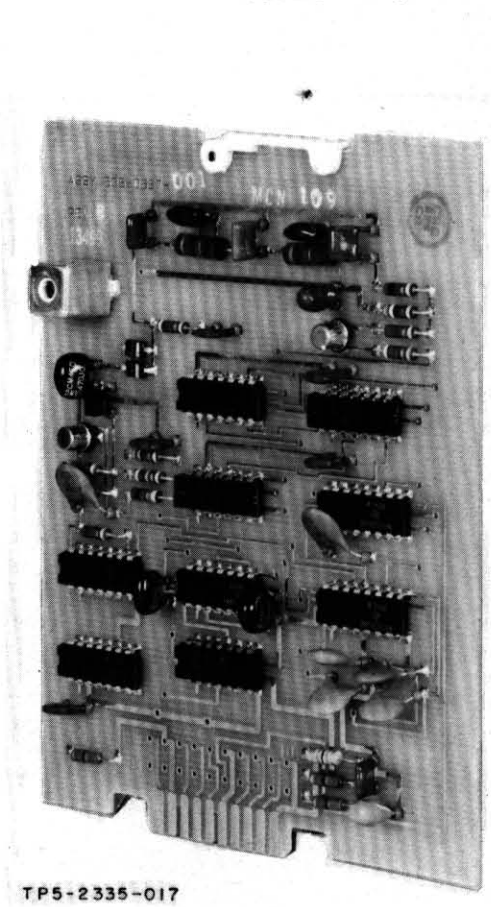
2. PRINCIPLES OF OPERATION

2.1 General (Refer to figure 2.)

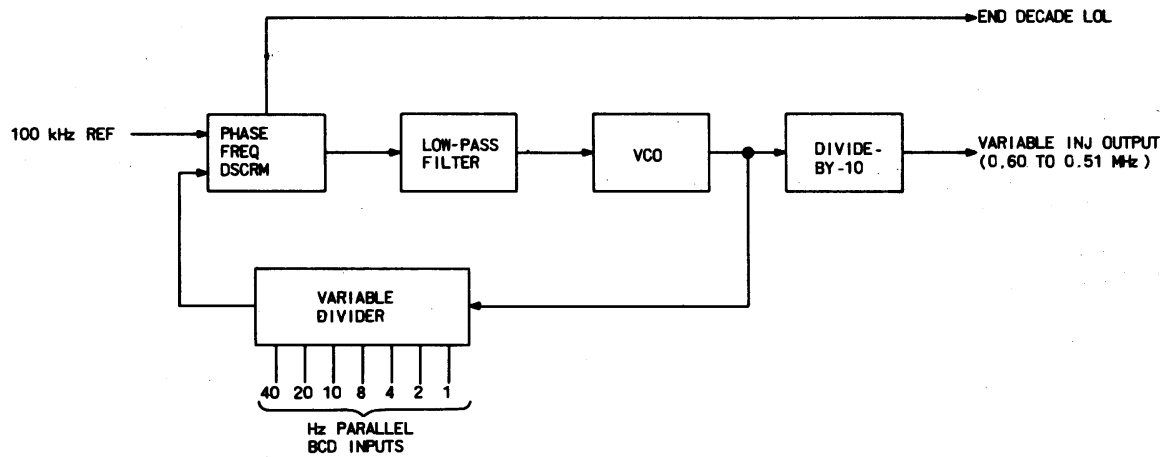
The synthesizer end decade receives 100/10/1-Hz bcd frequency control signals and a 100-kHz reference signal, and generates a 6.0- to 5.1-MHz variable frequency output and a lock signal output (logic 1 for lock).

The logic circuits receive a 100-kHz reference input and a bcd frequency input. The bcd frequency input is used to program a variable frequency divider (divide-by-60 to divide-by-51). The programmed variable divider output (100 kHz) and the 100-kHz reference input are supplied to a phase/frequency discriminator that provides a control voltage proportional to the phase/frequency difference between its inputs.

The vco circuit receives the control voltage signal from the logic circuits and is driven to and locked at the variable frequency as programmed by the variable divider bcd inputs to the logic circuits. The vco output (6.0 to 5.1 MHz) is supplied to the logic circuits for clocking and lock signal generation. The vco output (6.0 to 5.1 MHz) is supplied through a divide-by-10 circuit to rf circuits for additional frequency mixing and generation.



Synthesizer End Decade
Figure 1



Block Diagram
Figure 2

2.2 Logic Circuits

The logic circuits receive a 100-kHz reference input, a vco signal output, and bcd frequency inputs, and supplies a control voltage output signal to the vco.

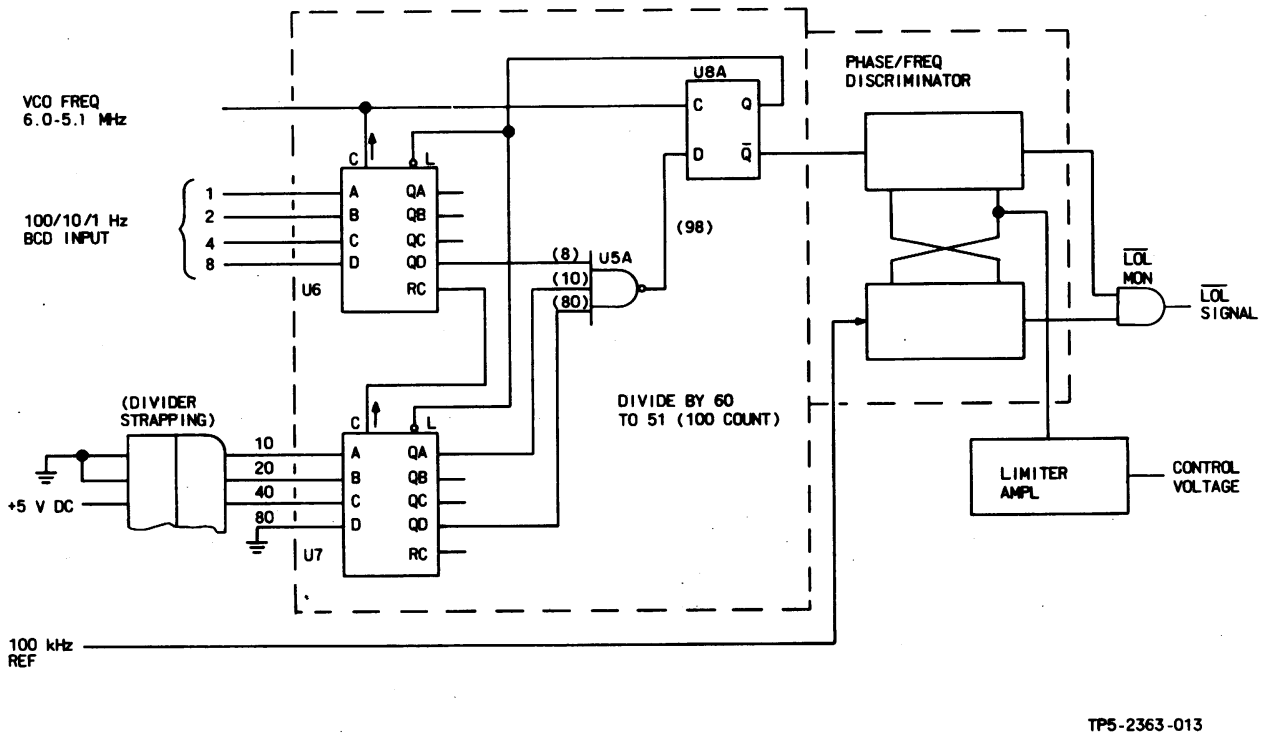
Refer to figure 3. The vco signal output (6.0 to 5.1 MHz) is supplied as the clock input to a programmable variable divider. The output of the programmable variable divider (100 kHz) is supplied to a phase/frequency discriminator and is compared with a 100-kHz reference input. A phase or frequency difference in the discriminator causes a control voltage input increase or decrease to adjust the frequency of the vco. If there is no phase or frequency difference, the discriminator provides a logic 1 lock signal output indicating the vco frequency is locked.

The programmable variable divider is programmed by the bcd frequency inputs. For example, if a bcd input of 0 is applied, the up/down decade counter is programmed to load the count 40 at any time a load signal (logic 0) is applied. Refer to table 1. This programs the variable divider to count from 40 (first count 41) to 100 (last count 100/40).

This causes the output of the variable divider to be 1/60th of the clock input or a divide-by-60 with a bcd input of 0. Note as the bcd input goes up 1, 2, 3, etc, the division ratio goes down -59, -58, -57, etc. Also note, that for the divide-by-circuit to operate as a constant, the last clock 100 must also be the loaded count (in the case of bcd 0, count 40). To do this, prerecognition of count 100 is required. Look-ahead circuit U5A performs this function. At clock 58 (count 98) gate U5A is NANDed and supplies a logic 0 input to U8A-D. With a logic 0 at U8A-D, clock 59 (count 99) causes U8A-Q to go to logic 1 and loads decade counter to bcd input (NANDed output of U5A is removed). At clock 59, U8A-$\overline{Q}$ supplies a pulse to phase/frequency discriminator. Clock 60 (count 40) causes U8A-Q to go to logic 0 and enables decade counter to count on the next clock. Next clock is one above the bcd programmed input. Note that count 99 initiates the output from the divider and count 100 appears only as the bcd programmed input. Refer to figure 4. A 500-Hz programmed input is shown, the same principles apply to any other programmed bcd input.

2.3 VCO Circuits

The vco circuits receive a control voltage from the logic circuits. The control voltage drives the vco to the required vco frequency. The vco signal output is supplied through one buffer amplifier to the logic circuits and through a fixed divide-by-10 output circuit to the unit under control for additional frequency mixing and generation.

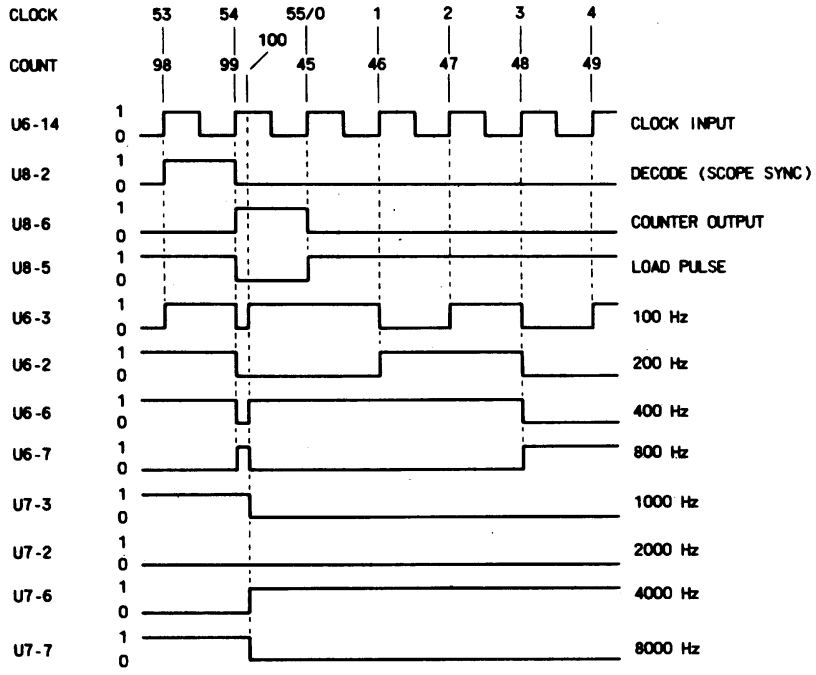


Logic Circuit
Figure 3

Table 1. Variable Divider, Logic Truth Table.

BCD INPUT (100/10/1 Hz)	DIVIDER INPUTS								OUTPUT COUNT	DIVIDE BY	LOOP FREQ (MHz)
	U6				U7						
	A	B	C	D	**A	**B	[1]C	*D			
0	0	0	0	0	0	0	1	0	40	60	6.0
1	1	0	0	0	0	0	1	0	41	59	5.9
2	0	1	0	0	0	0	1	0	42	58	5.8
3	1	1	0	0	0	0	1	0	43	57	5.7
4	0	0	1	0	0	0	1	0	44	56	5.6
5	1	0	1	0	0	0	1	0	45	55	5.5
6	0	1	1	0	0	0	1	0	46	54	5.4
7	1	1	1	0	0	0	1	0	47	53	5.3
8	0	0	0	1	0	0	1	0	48	52	5.2
9	1	0	0	1	0	0	1	0	49	51	5.1

*Internally strapped for logic 0 (ground).
**Externally strapped for logic 0 (ground) at pins 7 and 17.
[1]Externally strapped for logic 1 (+5.2 V dc) at pin 16.



PROGRAMMED BCD INPUTS		
MHz	PIN NO.	LOGIC LEVEL
1	U6-15	1
2	U6-1	0
4	U6-10	1
8	U6-9	0
10	U7-15	FXD 0
20	U7-1	FXD 0
40	U7-10	FXD 1
80	U7-9	FXD 0

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Variable Divider, Inputs and Outputs
Figure 4

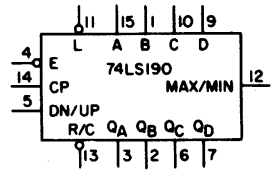
2.4 Up/Down Decade Counter 74LS190 (Refer to table 2.)

The 74LS190 up/down decade counter is a 4-bit decade counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when input conditions are met.

A high at the enable input inhibits counting. A low at the enable input and a low-to-high clock transition triggers the four master/slave flip-flops. The enable input should be changed only when the clock is high. The down/up input determines the direction of the count. When low, the count goes up; when high, the count goes down.

These counters are programmable. The outputs may be preset to any state by placing a low on the load input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the state of the clock input. This allows the counters to be used as modulo-N dividers by modifying the count length with the preset inputs.

Two outputs are available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high level output



V_{CC} = PIN 16
GND = PIN 8

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Up/Down Decade Counter 74LS190
Figure 5

pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low level output pulse equal in width to the low level portion of the clock input when an overflow or underflow condition exists. The counters are cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Table 2. Up/Down Decade Counter 74LS190, Logic Truth Table.

PROGRAMMABLE INPUTS				COUNT	BCD OUTPUTS			
A	B	C	D		QA	QB	QC	QD
0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	0	0	0
0	1	0	0	2	0	1	0	0
1	1	0	0	3	1	1	0	0
0	0	1	0	4	0	0	1	0
1	0	1	0	5	1	0	1	0
0	1	1	0	6	0	1	1	0
1	1	1	0	7	1	1	1	0
0	0	0	1	8	0	0	0	1
1	0	0	1	9	1	0	0	1

E (enable): logic 0 enables counter; logic 1 inhibits counter.

L (load): logic 0 programs the bcd output count to be set at the bcd count of the programmable inputs; the next clock pulse counts one higher/lower (up/down).

DU (down/up): logic 0 counts up; logic 1 counts down.

CP (clock pulse): logic 0-to-logic 1 transition advances counter.

RC (ripple clock): logic 0 pulse equal to 1/2 clock cycle when an overflow occurs.

MM (maximum/minimum count): logic 1 pulse equal to full clock cycle when an overflow or underflow occurs.

2.5 Decade Counter 74LS90 (Refer to table 3.)

The 74LS90 decade counter is a high-speed, monolithic decade counter consisting of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-2 counter and a divide-by-5 counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to a logical 0 or to a binary coded decimal (bcd) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated in three independent count modes:

a. When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the bcd count sequence truth table shown above. In addition to a conventional 0 reset, inputs are provided to reset a bcd 9 count for 9's complement decimal applications.

b. If a symmetrical divide-by-10 count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of 10, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-10 square wave is obtained at output A.

c. For operation as a divide-by-2 counter and divide-by-5 counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-2 function. The BD input is used to obtain binary divide-by-5 operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

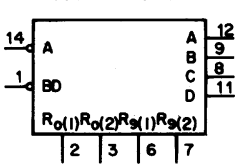
Table 3. Decade Counter 74LS90, Logic Truth Table.

*BCD COUNT SEQUENCE				
COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

**RESET/COUNT								
RESET INPUTS				OUTPUT				
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D	C	B	A	
1	1	0	X	0	0	0	0	
1	1	X	0	0	0	0	0	
X	X	1	1	1	0	0	1	
X	0	X	0	Count				
0	X	0	X	Count				
0	X	X	0	Count				
X	0	0	X	Count				

*Output A connected to input BD for BCD count.
**X indicates that either a logical 1 or a logical 0 may be present.

LOGIC SYMBOL



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Decade Counter 74LS90
Figure 6

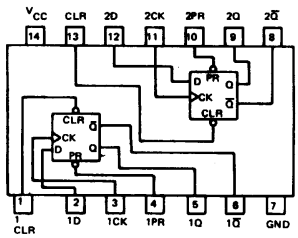
2.6 Dual D-Type Flip-Flop With Preset and Clear 74LS74 (Refer to table 4.)

The 74LS74 consists of dual, high-speed, D-type flip-flops. Information on the D input is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either high or low level, the D-input signal has no effect.

Table 4. Dual D-Type Flip-Flop With Preset and Clear 74LS74, Logic Truth Table.

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	*H	*H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q_0}$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated input conditions were established.
* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.



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Dual D-Type Flip-Flop With Preset and Clear 74LS74 Figure 7

3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the synthesizer end decade are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in table 5 check total performance of the synthesizer end decade. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.

Table 5. Synthesizer End Decade, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top cover of the unit containing the synthesizer end decade that is to be tested.		
	b. Remove cover from the synthesizer section of the unit.		
	c. Remove synthesizer end decade, install it on an extender card, and place it in the unit.		
	d. Set unit LINE SELECTOR switch to 115 V.		
(Cont)	e. Connect unit to 115-V ac power source and set power on.		

Table 5. Synthesizer End Decade, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. (Cont)	f. Measure dc voltage from P1-20 and P1-2 to P1-6 (ground).	+5.2 ±0.2 V dc.	Check unit synthesizer voltage regulator.
	g. Measure dc voltage from P1-10 to P1-6 (ground).	NLT +19.5 V dc, NMT +20.8 V dc.	Check unit synthesizer voltage regulator.
2. Test procedures	a. Set the end frequency control to 9.		
	b. Measure dc voltage at cathode end of CR1-CR2. (Refer to figure 8 for CR1-CR2 cathode location.)	9.5 ±0.1 V dc.	Adjust L6 for 9.5 ±0.1 V dc. If L6 adjustment does not correct the problem, check Q1, Q2, and associated circuit.
	c. Using a frequency counter, measure the output between P1-1 and P1-11 (ground).	510 ±0.5 kHz.	Adjust L6 for 510 kHz with 10.0 ±0.1 V dc at cathode end of CR1-CR2. If L6 adjustment does not correct the problem, check Q1, Q2, and associated circuit.
	d. Note the frequency counter reading while moving the frequency control from 9 down to 0. (Refer to chart below.)	Note that the frequency reading increases by 10 kHz with each step of the frequency control. Reading should be 600 ±0.5 kHz with frequency control at 0.	Check U6, U7, U8, and associated circuits.
	e. Measure the dc voltage at P1-12.	NLT +3.5 V dc. ***Note*** RCV FAULT, EXCTR FAULT, or R/E FAULT indicator lighting indicates that result of step f is satisfactory.	Check U3, U4, and U5.
(Cont)	f. Ground P1-5 while noting the voltage of P1-12.	NMT 0.5 V dc.	Check U1, U2, U3, U4, and U5.

Table 5. Synthesizer End Decade, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE		NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	g. Remove P1-5 ground.			
	LOW END FREQ DIGIT	CR1-CR2 DC VOLTAGE	FREQ OUTPUT P1-1 (kHz)	
	9	9.5 ±0.1	510 ±0.5	
	8	10.0 ±0.1	520 ±0.5	
	7	10.5 ±0.1	530 ±0.5	
	6	11.0 ±0.1	540 ±0.5	
	5	11.5 ±0.1	550 ±0.5	
	4	12.0 ±0.1	560 ±0.5	
	3	12.5 ±0.1	570 ±0.5	
	2	13.0 ±0.1	580 ±0.5	
	1	13.5 ±0.1	590 ±0.5	
	0	14.0 ±0.1	600 ±0.5	

4. ALIGNMENT/ADJUSTMENT

Refer to table 5 for adjustment of L6. Perform test 2, steps a through c.

5. REPAIR

Repair of the synthesizer end decade is accomplished using the standard planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

6. PARTS LIST/DIAGRAMS

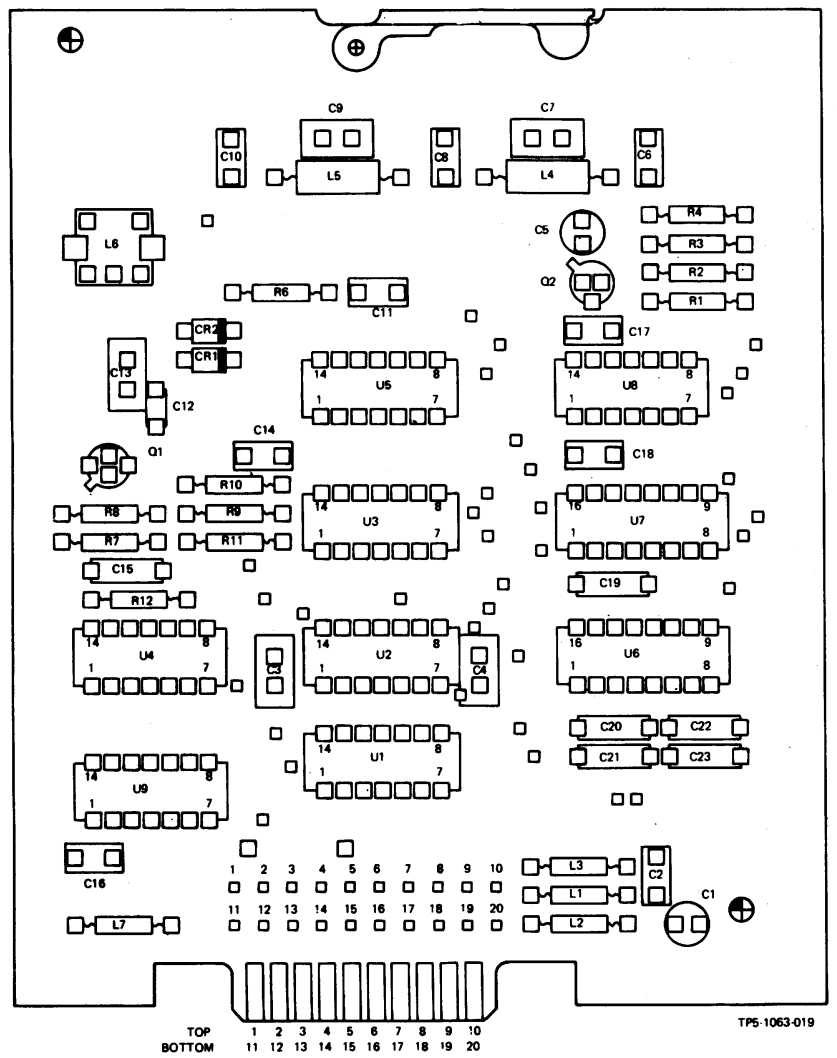
This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram, figure 8. The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

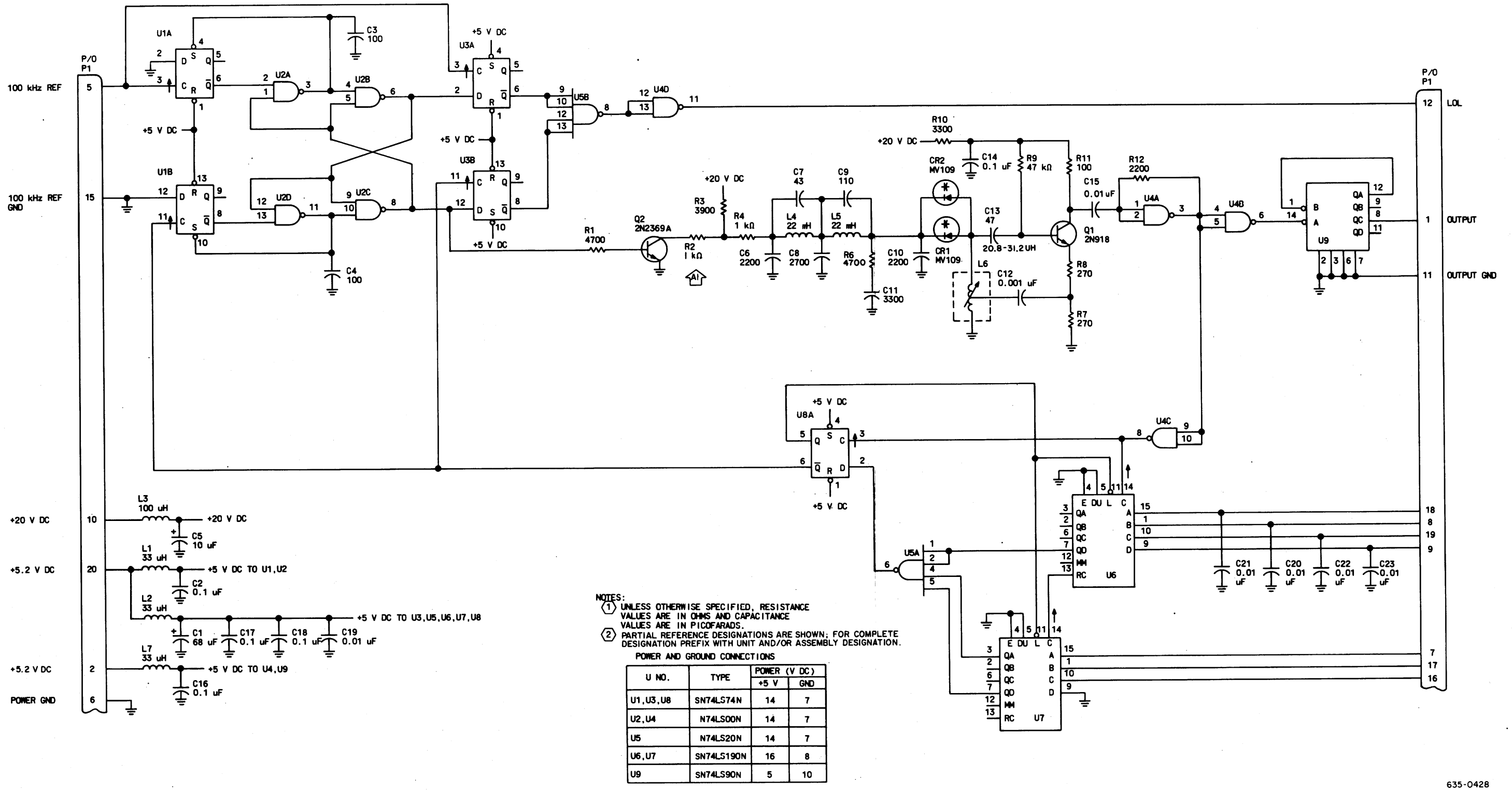
Use the reference designator indicated on schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description is listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points at the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Synthesizer end decade	635-0657-001	REV C





POWER AND GROUND CONNECTIONS

U NO.	TYPE	POWER (V DC)	
		+5 V	GND
U1,U3,U8	SN74LS74N	14	7
U2,U4	N74LS00N	14	7
U5	N74LS20N	14	7
U6,U7	SN74LS190N	16	8
U9	SN74LS90N	5	10

Synthesizer End Decade, Schematic Diagram
Figure 8 (Sheet 1 of 2)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	SYNTH END DECADE 635-0657-001		
CR1, CR2	SEMICOND DEVICE, MV109	922-6124-040	
C1	CAPACITOR, FXD, ELCTLT, 68μF, 20%, 6V	184-9102-040	
C2	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C3, C4	CAPACITOR, FXD, MICA DIEL, 100pF, 5%, 500V	912-3879-000	
C5	CAPACITOR, FXD, ELCTLT, 10μF, 20%, 25V	184-9102-240	
C6	CAPACITOR, FXD, CER DIEL, 2200pF, 5%, 100V	913-3281-300	
C7	CAPACITOR, FXD, MICA DIEL, 43pF, 5%, 500V	912-3854-000	
C8	CAPACITOR, FXD, CER DIEL, 0.0027μF, 5%, 100V	913-3117-130	
C9	CAPACITOR, FXD, MICA DIEL, 110pF, 5%, 500V	912-3882-000	
C10	CAPACITOR, FXD, CER DIEL, 2200pF, 5%, 100V	913-3281-300	
C11	CAPACITOR, FXD, CER DIEL, 3300pF, 10%, 100V	913-3281-170	
C12	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C13	CAPACITOR, FXD, MICA DIEL, 47pF, 5%, 500V	912-3856-000	
C14	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C15	CAPACITOR, FXD, CER DIEL, 0.01μF, -20%+80%, 100V	913-3680-000	
C16-C18	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C19-C23	CAPACITOR, FXD, CER DIEL, 0.01μF, -20%+80%, 100V	913-3680-000	
L1, L2	COIL, RF, 33μH	240-2041-000	
L3	COIL, RF, 100μF	240-2047-000	
L4, L5	COIL, RF, 22000 μH	240-2715-650	
L6	INDUCTOR, RF, VAR, 20.8-31.2μH	242-0441-050	
L7	COIL, RF, 33μH	240-2041-000	
Q1	TRANSISTOR, 2N918	352-0440-000	
Q2	TRANSISTOR, 2N2369A	352-0596-030	
R1	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R2	RESISTOR, FXD, CMPSN, 2.2kΩ, 10%, 1/4W (A1)	745-0761-000	
R2	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/4W (A1)	745-0749-000	
R3	RESISTOR, FXD, CMPSN, 3.9kΩ, 10%, 1/4W	745-0770-000	
R4	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/4W	745-0749-000	
R5	NOT USED		
R6	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R7, R8	RESISTOR, FXD, CMPSN, 270Ω, 10%, 1/4W	745-0728-000	
R9	RESISTOR, FXD, CMPSN, 47kΩ, 10%, 1/4W	745-0809-000	
R10	RESISTOR, FXD, CMPSN, 3.3kΩ, 10%, 1/4W	745-0767-000	
R11	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/4W	745-0713-000	
R12	RESISTOR, FXD, CMPSN, 2.2kΩ, 10%, 1/4W	745-0761-000	
U1	INTEGRATED CKT, SN74LS74N	351-1525-040	
U2	INTEGRATED CKT, N74LS00N	351-1523-110	
U3	INTEGRATED CKT, SN74LS74N	351-1525-040	
U4	INTEGRATED CKT, N74LS00N	351-1523-110	
U5	INTEGRATED CKT, N74LS20N	351-1523-130	
U6, U7	INTEGRATED CKT, SN74LS190N	351-1527-040	
U8	INTEGRATED CKT, SN74LS74N	351-1525-040	
U9	INTEGRATED CKT, SN74LS90N	351-1636-010	

MODIFICATION HISTORY

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A1	Changed R2 from 2200Ω to 1kΩ.	REV C and above

Synthesizer End Decade, Schematic Diagram
Figure 8 (Sheet 2)